

1 96. The method of making the multi-layered interconnect structure of claim 91 further  
2 including the steps of:

3 positioning a fourth dielectric layer on said second dielectric layer and on said second  
4 plurality of electrically conductive members;

5 removing portions of said fourth dielectric layer to expose portions of said second  
6 plurality of electrically conductive members; and

7 forming a second plurality of microvias within said fourth dielectric layer to expose at  
8 least a portion of at least one of said second plurality of electrically conductive  
9 members.

10 97. The method of making the multi-layered interconnect structure of claim 96 wherein  
11 the step of removing portions of said fourth dielectric layer is performed by laser  
12 ablating.--

13 A2 concluded

14 REMARKS

15 The specification is amended to reference the parent application, S/N 09/346,356.

16 Claims 1-79 are cancelled. Claims 80-97, directed to Applicant's method, and  
17 withdrawn in the parent application, have been added.

18 New independent method claim 80 recites the subject matter of original independent  
19 method claim 69.

New dependent method claims 81-86 recite the subject matter of original dependent claims 70-75, and depend from new independent claim 80.

New independent method claim 87 recites the subject matter of original independent claim 76. New dependent claims 88-90 recite the subject matter of original dependent claims 77-79 and depend from new independent method claim 87.

New independent method claim 91 recites the subject matter of original independent method claim 69 and includes the steps of positioning a first electrically conductive layer within the first dielectric layer, and positioning a second electrically conductive layer between the first electrically conductive layer and the thermally conductive layer wherein the second electrically conductive layer comprises a first plurality of shield signal conductors. Support is found on page 7, lines 10-17 and lines 23-24.

New dependent method claims 92-97 recite the subject matter of original dependent claims 70-75 and depend from new independent method claim 91.

Support being provided for all the above amending, this amending does not constitute the addition of new matter and entry is urged.

Attached hereto is a marked up version of the changes made to the specification by the current amendment. This page is captioned Version with markings to show changes made.

Copies of the IDS and PTO-1449 form mailed on 08/12/99 and Supplemental IDS and PTO-1449 forms mailed on 09/29/99, 07/05/00, and 08/21/01 in the parent application, S.N. 09/346,356, are included herewith. Upon request, copies of the documents cited in the IDSs and PTO-1449 forms will be provided.

The Application is deemed in condition for allowance and such action by the Examiner is urged. Should differences remain, however, which do not place one/more of the remaining claims in condition for allowance, the Examiner is requested to phone the undersigned at the number provided below for the purpose of providing constructive assistance and suggestions in accordance with M.P.E.P. Sections 707, 707.07(d) and 707.07(j) in order that allowable claims can be presented, thereby placing the application in condition for allowance without further proceedings being necessary.

Respectfully submitted,

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ELECTRONIC PACKAGE FOR ELECTRONIC  
COMPONENTS AND METHOD OF MAKING SAME

TECHNICAL FIELD

The present invention relates, in general, to an electronic package for mounting of  
5 integrated circuits, and in particular, to an organic multi-layered interconnect structure for use in  
such a package.

Added "Cross Reference to Copending Application"

BACKGROUND OF THE INVENTION

10040745-01015  
20010524001  
Organic substrates for example printed circuit boards and chip carriers have been and  
continue to be developed for many applications. These are expected to displace ceramic  
substrates, in particular in many chip carrier applications, because of reduced cost and enhanced  
electrical performance. The use of a multi-layered interconnect structure such as an organic chip  
carrier for interconnecting a semiconductor chip to a printed circuit board in an electronic  
package introduces many challenges, one of which is the reliability of the connection joints  
between the semiconductor chip and the organic chip carrier and another of which is the  
reliability of the connection joints between the organic chip carrier and the printed circuit board.

20 As semiconductor chip input/output (I/O) counts increase beyond the capability of  
peripheral lead devices and as the need for both semiconductor chip and printed circuit board  
miniaturization increases, area array interconnects are the preferred method for making large  
numbers of connections between a semiconductor chip and an organic chip carrier and between  
the organic chip carrier and a printed circuit board. If the coefficient of thermal expansion (CTE)  
of the semiconductor chip, the organic chip carrier, and the printed circuit board are substantially  
different from one another, industry standard semiconductor chip array interconnections to the  
organic chip carrier can exhibit high stress during operation (thermal cycling). Similarly, the  
industry standard ball grid array (BGA) interconnections between the organic chip carrier and